User's and Programming Guide

Agilent Technologies
ESG Family Signal Generators
Option UN7 Bit Error Rate Test

Agilent Technologies

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1 The Bit Error Rate Test

This guide describes features specific to the bit error rate test (BERT) capability of the Agilent Technologies ESG Family Signal Generator with Option UN7.

Overview

The bit error rate test (BERT) function allows you to test the bit error rate (BER) of digital communications equipment, such as sensitivity and selectivity of receivers or components.

This document contains the following chapters:

Chapter 1, "The Bit Error Rate Test," briefly explains the contents of this document.

Chapter 2, "Using Functions," shows an example of typical operating procedures to make a BER measurement on a radio.

Chapter 3, "Reference," describes the principal operation of the softkeys, display annotation, and the rear panel connectors which are implemented for the BERT function.

Chapter 4, "Operation," explains some unique BERT features which might be beneficial to users.

Chapter 5, "Remote Programming," contains a brief overview of the Standard Commands of Programmable Instruments (SCPI) programming language and an alphabetical listing of all of the SCPI commands which are implemented for the BER measurement function.

Chapter 6, "Programming Command Cross-Reference," lists all of the BERT softkeys and their corresponding SCPI commands.

Chapter 7, "Programming Examples," shows a list of the programming statements to make a typical BER measurement on a radio.

This guide is only for Option UN7. Refer to the user's guide and/or programming guide for the ESG Family Signal Generator for general functions such as setting the frequency and amplitude of the RF output.

NOTE One of the I/Q baseband generator options is required to operate Option UN7. This manual documents use with Option UN8.

Verifying Bit Error Rate Test Operation

The operator's check is appropriate as a daily functional check, or whenever the integrity of the bit error rate test function is in question. Use the operator's check to verify proper operation of the bit error rate test function. The operator's check does not ensure performance to specifications.

Operator's Check

Perform the following tasks in order:

1. Connect the cables between the rear panel connectors as follows:
   - DATA OUT to BER DATA IN
   - DATA CLK OUT to BER CLK IN

   Use the BNC-BNC cables, or the SMB-SMB cables if the signal generator is equipped with Option 1EM.
2. Press the **Preset** key to preset the signal generator to the normal preset conditions.
3. Press the **Mode** key. Then, if you have multiple options and the **Real Time I/Q BaseBand** softkey is visible, press it next. Then press **TDMA** > **PHS**. Now set these softkeys as follows:
   - **PHS Off On** to **On**
   - **Data Format Pattern Framed** to **Pattern**
   - **Data** to **PN9**
4. Press **Mode** > **BERT**. Set the softkeys as follows:
   - **BERT Off On** to **On**
   - **Display BER % Exp** to **%**
   - **Display Update Cycle End Cont** to **Cont**
5. Press **Configure BERT**. Set the softkeys as follows:
   - **Max. Data Rate 2Mbps 10Mbps** to **2Mbps**
   - **Total Bits** to **100 000**
   - **Special Pattern Ignore Off On** to **Off**
6. Press **More (1 of 3)**. Set the softkeys as follows:
   - **BERT Resync Off On** to **Off**
   - **Pass/Fail Off On** to **Off**

7. Press **More (2 of 3)**. Set the softkeys as follows:
   - **Clock Polarity Pos Neg** to **Neg**
   - **Data Polarity Pos Neg** to **Pos**
   - **Clock Gate Off On** to **Off**
   - **Impedance 75 Ohm TTL** to **TTL**
8. Press **Return** > **Configure Trigger**. Set the softkeys as follows:
   - **BERT Trigger** to **Immediate**
   - **Cycle Cont** to **0**
   - **Bit Delay Off On** to **Off**
9. You will see the following results on the display:

Total Bits	Error Bits	BER
0 to 100,000 bits	0 bits	0.00000000%
(counting up)	(always)	(always)

10. Disconnect the cable between the DATA OUT connector and the BER DATA IN connector. Notice the `No Data` annunciator on the lower left corner of the display. This annunciator turns off when you reconnect the cable.
11. Disconnect the cable between the DATA CLK OUT connector and the BER CLK IN connector. Notice the `No Clock` annunciator on the lower left corner of the display. This annunciator turns off when you reconnect the cable, and the BER result is almost 50%.

    Press the **Return** key and toggle the **BERT Off On** softkey to **Off** and then to **On**. You will see the new BER result is the same as shown in the table above.
12. Press **Configure BERT** > **More (1 of 3)** > **More (2 of 3)**. Toggle the **Clock Gate Off On** softkey to **On** and the **Clock Gate Polarity Pos Neg** softkey to **Pos**. You will see the same display as shown in the table above.

    Change **Clock Gate Polarity Pos Neg** to **Neg** and you will see `Sync Loss` and `No Clock` on the lower left corner of the display.

    Connect a short connector to the rear panel BER GATE IN connector and you will observe a new BER measurement is being done.

2 Using Functions

This chapter contains procedures to show you how to use some of the major functions of the Bit Error Rate Test (BERT).

Setting Up a Bit Error Rate Test on a PHS radio

Use this procedure to make BER measurements on a PHS radio with the Agilent Technologies ESG-D and ESG-DP Series Signal Generator with Option UN7. This section explains each of the following objectives:

- making the cable connections
- setting the carrier frequency and the power level
- selecting the PHS data format
- setting the PHS radio to a receiver mode
- selecting the BERT data pattern to PN9, maximum data rate to 2 Mbps, and total bits to 100,000
- selecting the BERT trigger
- starting the BERT measurements

Making the Cable Connections

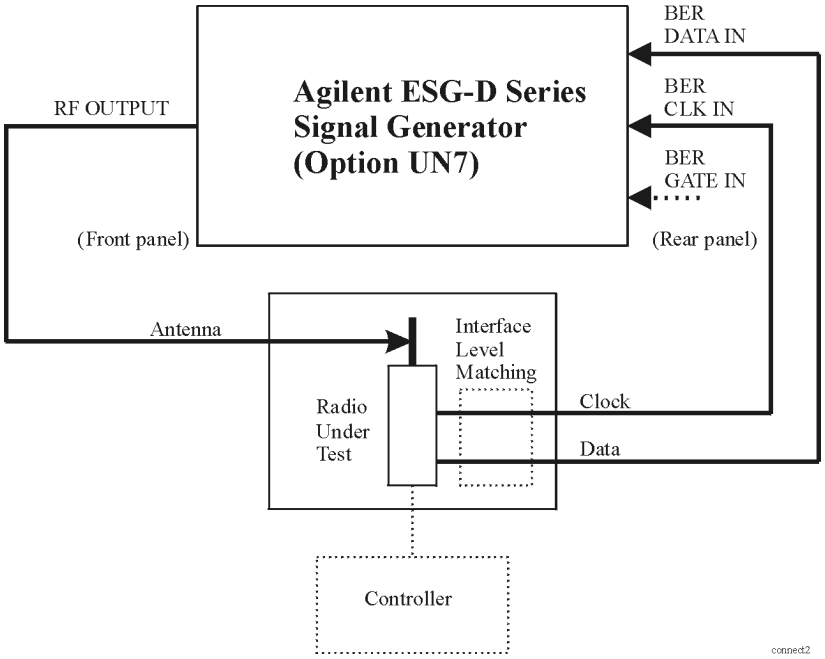
1. Connect the cables between your radio and the ESG-D and ESG-DP Series Signal Generator with Option UN7 as follows:

	ESG-D and ESG-DP Series Signal Generator Option UN7[1]	**Radio**
RF signal:	RF OUTPUT connector (front panel[2])	Antenna Input port
Data signal:	BER DATA IN connector (rear panel)	Data Output port
Clock signal:	BER CLK IN connector (rear panel)	Clock Output port

1. In this example, the BER GATE IN connector is not used.
2. Rear panel, when the signal generator is equipped with Option 1EM.

An external controller will be required to control the radio under test. An interface level matching circuit will be required for interfacing between the radio under test and the ESG-D and ESG-DP Series Signal Generator with Option UN7, when the radio signal specifications are different from those of the signal generator.

Figure 2-1 Test Setup for a Bit Error Rate Test



Setting the Carrier Frequency and Power Level

1. Press the front panel **Preset** key to preset the signal generator to the normal preset conditions.
2. Press the front panel **Frequency** key. Frequency becomes the active function and the normal preset value for frequency is displayed in the active entry area.

   Enter the carrier frequency (for example, 1.89515 GHz) using the numeric keypad and pressing one of the terminator softkeys. The new carrier frequency is shown in the frequency area of the display.
3. Press the front panel **Amplitude** key. Amplitude becomes the active function and the normal preset value for amplitude is displayed in the active entry area.

   Enter the power level (for example, –100 dBm) using the numeric keypad and pressing one of the terminator softkeys. The new power level is shown in the amplitude area of the display.

Selecting the Radio Data Format

1. Press the front panel **Mode** key. Then, if you have multiple options and the **Real Time I/Q BaseBand** softkey is visible, press it next. Then press **TDMA** and the **PHS** softkey to select the PHS communications standard.
2. Toggle the **Data Format Pattern Framed** softkey to **Framed**. When you select **Framed** for bursting the frame envelope, you will be transmitting framed data. This means that you will be bursting the timeslots that you have activated and there will be no RF carrier during the off timeslots. Notice that the **Configure Timeslots** softkey has become an active softkey.
3. Observe the display and notice that the normal preset condition for downlink timeslot #1 has the timeslot turned on and configured as a traffic channel (TCH). Press the **Configure Timeslots** softkey and look at the softkeys. The **Timeslot #** softkey shows that downlink timeslot #1 is selected as the active timeslot. The **Timeslot Off On** softkey shows that downlink timeslot #1 is turned on. The **Timeslot Type** softkey shows that downlink timeslot #1 is configured as a traffic channel. Press the **Configure TCH** softkey. The **Data** softkey shows that PN9 is selected as a data pattern.
4. Press the front panel **Return** key to move up the softkey menus until the first PHS menu is displayed. (The first softkey in this menu is **PHS Off On**.) Press the **PHS Off On** softkey to toggle the PHS format from **Off** to **On**. At this time the internal baseband generator will generate the internal data patterns that you have configured for Downlink timeslot 1 and Uplink timeslot 1. A message is displayed while this process is taking place. Notice, also, that the PHS, I/Q, and ENVLP display annunciators are turned on.
5. Press the front panel **RF On/Off** key to toggle RF on. Notice that the display annunciator changes from RF OFF to RF ON. The modulated signal is now available at the RF OUTPUT connector.

Setting the Radio to a Receiver Mode

Set the PHS radio to receive the signal of the specified carrier frequency and the timeslot 1, and output the data used for the bit error rate measurements.

Selecting the BERT Data Pattern, Maximum Data Rate, and Total Bits

1. Press the **Mode** key and then press the **BERT** softkey to configure parameters for making BER measurements.
2. Press the **Configure BERT** softkey and look at the softkeys. The **Data** softkey shows that PN9 is selected as the data pattern. The **Max. Data Rate 2Mbps 10Mbps** softkey shows that the maximum data rate is set to 2 Mbps mode.
3. Press the **Total Bits** softkey and enter 100,000 in this entry field using the numeric keypad and pressing **Bits** terminator softkey.

Selecting the BERT Trigger

1. Press the **Return** key once to move up one level of softkey menus until the first BERT menu is displayed. (The first softkey in this menu is **BERT Off On**.)
2. Press the **Configure Trigger** softkey to reveal the next menu.
3. Notice that the Trigger Key is active in the **BERT Trigger** softkey as the default setting.
4. Press the **Return** key once to move up one level of softkey menus until the first BERT menu is displayed. (The first softkey in this menu is **BERT Off On**.) Press the **BERT Off On** softkey. The BERT toggles from **Off** to **On**.

Starting BERT measurements

1. Press the front panel **Trigger** key for starting a BER measurement. You will see the measurement result values of the Total Bits, Error Bits, and BER on the display.

NOTE If you encounter difficulty making a BER measurement, check the following:

- Make sure that the cable connections are properly configured.
- Make sure the data pattern for the BER measurement, specified by the **Data** softkey, matches the data pattern in the traffic channel (TCH) for the RF signal being input to the radio under test.
- Make sure RF is turned on.
- Make sure the amplitude is set to the correct level.
- Make sure if the radio under test is controlled to receive the signal of the specified carrier frequency and the timeslot.

3 Reference

This chapter contains descriptions for each softkey, the display annotations, and the rear panel connectors that are specific to your Agilent Technologies ESG Family Signal Generator with Option UN7.

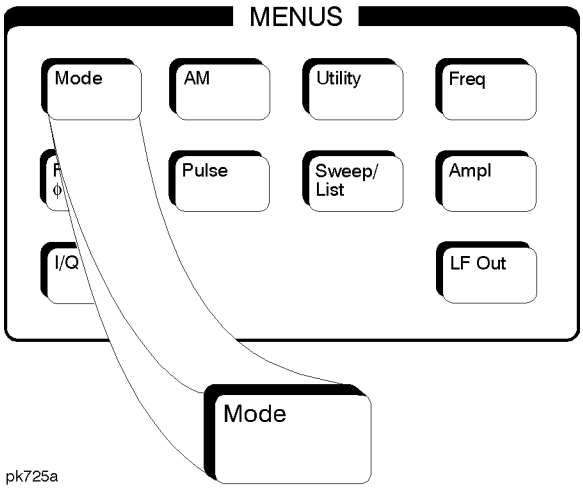
For information and guidance on how to operate these functions remotely, see Chapter 5, “Remote Programming” and Chapter 6, “Programming Command Cross-Reference.”

Softkey Reference

The following section describes briefly the **Mode** key, and explains the associated softkeys that are used to activate functions specific to the bit error rate test (BERT).

Mode Key

Pressing the front panel **Mode** key accesses a menu of softkeys. These softkeys let you access further menus for configuring the digital modulation formats. The Option UN7 signal generator has one more selection in this menu: **BERT**. The BERT selection provides the softkeys which allow you to set parameters to make bit error rate (BER) measurements.



BERT

Press this softkey to access a menu of softkeys for setting or specifying all of the parameters required to make BER measurements. These softkeys are described in this section in alphabetical order.

BERT Off On

Press this softkey to enable and disable the BER measurement function.

Default value: Off

Softkey Location: **Mode** > **BERT** > **BERT Off On**

BERT Resync Off On

Sets the operating state of the resynchronizing function. This softkey is valid only when the **Max. Data Rate 2Mbps 10Mbps** softkey is already set to **2Mbps**. When you select **On**, a new BER measurement will immediately be restarted whenever the previous BER measurement result exceeds the value specified by the **Resync Limits** softkey.

Default value: On

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Max. Data Rate 2Mbps** > **BERT Resync Off On**

BERT Trigger

Accesses a menu of choices for triggering BER measurements. You can choose triggering that occurs immediately (**Immediate**), triggering by the front panel **Trigger** key (**Trigger Key**), triggering that is supplied by the GPIB (**Bus**), or triggering on the positive edge of a signal supplied to the TRIGGER IN connector (**Ext**).

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **BERT Trigger**

Bus

This softkey is one of the choices in the BERT Trigger menu. With **Bus** selected, use the `*TRG` GPIB command to trigger BER measurements.

Default value: BERT trigger is set to Trigger Key

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **BERT Trigger** > **Bus**

Clock Gate Off On

Toggles the clock gate function off and on. When you select **On**, the clock signal is valid when the clock gate signal is high for the normal (positive) mode, or low for the inverted (negative) mode. This clock gate signal is connected to the rear panel BER GATE IN connector.

Default value: Off

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Clock Gate Off On**

Clock Gate Polarity Neg Pos

Inputs polarity of the clock gate signal supplied to the rear panel BER GATE IN connector. When you select **Pos** (positive), the clock signal is valid when the clock gate signal is high; when you select **Neg** (negative), the clock signal is valid when the clock gate signal is low.

Default value: Pos (Positive)

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Clock Gate On** > **Clock Gate Polarity Neg Pos**

Clock Polarity Neg Pos

Inputs polarity of the clock signal supplied to the rear panel BER CLK IN connector. When you select **Pos** (positive), the rising edge is used; when you select **Neg** (negative), the falling edge is used.

Default value: Pos (Positive)

Softkey Location: **Mode** > **BERT** > **Configure BERT** >**Clock Polarity Neg Pos**

Configure BERT

Accesses more menus for configuring test parameters for BER measurements.

Softkey Location: **Mode** > **BERT** > **Configure BERT**

Configure Trigger

Accesses more menus for configuring trigger parameters for BER measurements.

Softkey Location: **Mode** > **BERT** > **Configure Trigger**

Cycle Count

Specifies the number of repetitions of BER measurements. The range of the acceptable values is from 0 to 65,535. With 0 set, the BER measurements are repeated till you set the **BERT Off On** softkey to **Off**. Enter the value using the numeric keypad and terminate it by pressing the **Enter** softkey.

Default value: 1

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **Cycle Count**

Cycle End

This softkey is one of the choices in the Pass/Fail Update menu. With **Cycle End** selected, a pass or fail judgement is made for each BER measurement result.

Default value: Pass/Fail Update mode is Cycle End

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Pass/Fail On** > **Pass/Fail Update** > **Cycle End**

Data

Press this softkey to access a menu of choices for the incoming data pattern to the BER DATA IN connector with either PN9 or PN15.

NOTE Be sure to match this value to the data pattern in the traffic channel (TCH) of the RF signal which is input to the radio under test.

Default value: PN9

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Data**

Data Polarity Neg Pos

Press this softkey to set the input polarity of the data signal supplied to the rear panel BER DATA IN connector. When you select **Pos** (positive), the data signal is used as it is; when you select **Neg** (negative), the polarity of the data signal is inverted.

Default value: Pos (Positive)

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Data Polarity Pos Neg**

Delayed Bits

Press this softkey to specify the number of delay bits from the trigger event for starting BER measurements. This softkey is valid only when the **BERT Trigger Bit Delay** softkey is set to **On**. The acceptable range of values is from 0 to 65,535. Enter the value using the numeric keypad and terminate it by pressing the **Enter** softkey.

Default value: 0

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **Bit Delay On** > **Delayed Bits**

Display BER % Exp

Sets the display mode for BER measurement results. When you select **%**, the BER measurement results are displayed in percent. When you select **Exp**, the BER measurement results are displayed in the exponential format of n.nnnnnE-mm.

Default value: %

Softkey Location: **Mode** > **BERT** > **Display BER % Exp**

Display Update Cycle End Cont

Displays update mode during BER measurements. When you select **Cycle End**, the previous BER measurement result is displayed during the current measurement cycle. When you select **Cont**, the display shows its real-time intermediate results during each BER measurement. This softkey is valid only when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps.**

Default value: Cycle End

Softkey Location: **Mode** > **BERT** > **Display Update Cycle End Cont**

Ext

With **Ext** selected, BER measurements are made by the external trigger signal supplied to the rear panel TRIGGER IN connector.

Default value: BERT trigger is set to Trigger Key

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **BERT Trigger** > **Ext**

Fail Hold

This softkey is one of the choices in the Pass/Fail Update menu. With **Fail Hold** selected, the fail judgement is made once fail has been found during one loop of BER repeat measurements.

Default value: Pass/Fail Update mode is set to Cycle End

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Pass/Fail On** > **Pass/Fail Update** > **Fail Hold**

Immediate

This softkey is one of the choices in the BERT Trigger menu. With **Immediate** selected, BER measurements are initiated and repeated until you set the **BERT Off On** softkey to **Off** or until you set the **BERT Trigger** softkey to **Trigger Key**, **Bus**, or **Ext.**

Default value: BERT trigger is set to Trigger Key

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **BERT Trigger** >**Immediate**

Impedance 75 Ohm TTL

Sets the input termination mode of the rear panel BER DATA IN, BER CLK IN, and BER GATE IN connectors.

Default value: TTL

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Impedance 75 Ohm TTL**

Max. Data Rate 2Mbps 10Mbps

Sets the maximum data bit rate mode of BER measurements. When you select **2Mbps**, all of the functions can be activated for BER measurements. When you select **10Mbps**, the resynchronization and special pattern ignore functions are not available, and you can not set the **Display Update Cycle End Cont** softkey to **Cont**.

Default value: 2Mbps

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Max. Data Rate 2Mbps 10Mbps**

Pass/Fail Limits

Specifies the threshold level of the comparator function. The range of the variable is from 0.0000001 (0.1ppm) to 1.0000000 (100%). Enter the value using the numeric keypad and terminate it by pressing the **%** or **ppm** softkey.

Default value: 0.0100000 (1%)

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Pass/Fail On** > **Pass/Fail Limits**

Pass/Fail Off On

Toggles the pass/fail judgement function off and on. The pass/fail judgement function compares a BER measurement result with the threshold level defined by the **Pass/Fail Limits** softkey, and judges whether that BER measurement result has passed or failed.

Default value: Off

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Pass/Fail Off On**

Pass/Fail Update

Accesses the pass/fail judgement update mode menu. With **Cycle End** selected, either pass or fail judgement is made for each BER measurement result. With **Fail Hold** selected, the fail judgement is made once fail has been found during one loop of BER repeat measurements.

Default value: Cycle End

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Pass/Fail On** > **Pass/Fail Update**

PN9

This softkey is one of the choices in the Data Select menu. With **PN9** selected, the incoming data to the BER DATA IN connector is assumed to be PN9 data.

Default value: Data is set to PN9

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Data** > **PN9**

PN15

This softkey is one of the choices in the Data Select menu. With **PN15** selected, the incoming data to the BER DATA IN connector is assumed to be PN15 data.

Default value: Data is set to PN9

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Data** > **PN15**

Resync Limits

Press this softkey to specify the threshold level for resynchronizing BER measurements. This softkey is valid only when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps** and the **BERT Resync Off On** softkey is set to **On**. The acceptable range of values is from 0.0500 to 0.4000. Enter the value using the numeric keypad and terminate it by pressing the **%** or **ppm** softkey.

Default value: 0.4000

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Max. Data Rate 2Mbps** > **BERT Resync On** > **Resync Limits**

Special Pattern 0's 1's

Press this softkey to set the parameter of the special pattern ignore function. With 0's selected, more than 80 bits of 0's are ignored when they are detected. With 1's selected, more than 80 bits of 1's are ignored when they are detected. This softkey is valid only when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps** and the **Special Pattern Ignore Off On** softkey is set to **On**.

Default value: 0's

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Max. Data Rate 2Mbps** > **Special Pattern Ignore On** > **Special Pattern 0's 1's**

Special Pattern Ignore Off On

Press this softkey to set the operating state of the special pattern ignore function. This function detects more than 80 bits of 0's or 1's in the incoming bit stream and ignores these bits during BER measurements. This softkey is valid only when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps**.

Default value: Off

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Max. Data Rate 2Mbps** > **Special Pattern Ignore Off On**

Total Bits

Press this softkey to specify the total bit count to be measured for one measurement cycle. The acceptable range of values is from 100 to 4,294,967,295. Enter the value using the numeric keypad and terminate the value by pressing the **Bits**, **KBits**, **10KBits**, **100KBits**, **MBits**, **10MBits**, or **100MBits** softkey.

Default value: 10,000

Softkey Location: **Mode** > **BERT** > **Configure BERT** > **Total Bits**

Trigger Key

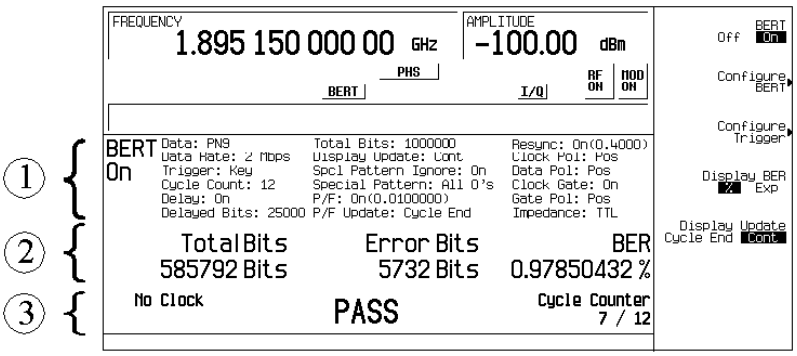
This softkey is one of the choices in the BERT Trigger menu. With **Trigger Key** selected, BER measurements are made by pressing the front panel **Trigger** key.

Default value: BERT trigger is set to Trigger Key

Softkey Location: **Mode** > **BERT** > **Configure Trigger** > **BERT Trigger** > **Trigger Key**

Display Annotation

The following figure shows the display graphics that appear when the BERT menu is accessed:



display

1. Setting Information

In this area, the setting information of the bit error rate tests are displayed.

- `BERT ON` - Indicates that the bit error rate test (BERT) is enabled. This field changes to `BERT OFF` when the **BERT Off On** softkey is set to **Off**.
- `Data: PN9` - Indicates that a PN9 sequence has been selected for an incoming data pattern. This field changes to `PN15` when the **Data** softkey is set to **PN15**.
- `Data Rate: 2 Mbps` - Indicates that the 2 Mbps mode has been selected for the maximum data rate. This field changes to `Data Rate: 10 Mbps` when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **10Mbps**.
- `Trigger: Key` - Indicates that the front panel **Trigger** key has been selected for a BERT trigger source. Other selections for the trigger field include `Bus`, `Ext`, and `Imm` (Immediate) depending on your **BERT Trigger** softkey setting.
- `Cycle Count: 12` - Indicates the number of repetitions of BER measurement cycles.
- `Delay: On` - Indicates that the trigger delay is enabled. This field changes to `Delay: Off` when the **Bit Delay Off On** softkey is set to **Off**.
- `Delayed Bit: 25000` - Indicates the number of delay bits from the trigger event for starting BER measurements. The grey text in this field indicates an inactive function (the trigger delay is disabled).

- `Total Bits: 100000` - Indicates the total bit count to be measured for one measurement cycle.
- `Display Update: Cont` - Indicates that the continuous mode has been selected for the display update mode. This field changes to `Display Update: Cycle End` when the **Display Update Cycle End Cont** softkey is set to **Cycle End**.
- `Spcl Pattern Ignore: On` - Indicates that the special pattern ignore is enabled. This field changes to `Spcl Pattern Ignore: Off` when the **Special Pattern Ignore Off On** softkey is set to **Off**.
- `Special Pattern: All 0's` - Indicates that the All 0's data pattern is selected for special pattern ignore function. This field changes to `Spcl Pattern Ignore: All 1's` when the **Special Pattern 0's 1's** softkey is set to **1's**. The grey text in this field indicates an inactive function (the special patter ignore function is disabled).
- `P/F: On(0.0100000)` - Indicates that the pass/fail judgement is enabled and its threshold level is set to 0.0100000. This field changes to `P/F Off` when the **Pass/Fail Off On** softkey is set to **Off** and the number in parentheses changes to display whatever value is set for the **Pass/Fail Limit** softkey.
- `P/F Update: Cycle End` - Indicates that the cycle end mode has been selected for the pass/fail judgement update mode. This field changes to `Display Update: Fail Hold` when **Fail Hold** is selected for the **Pass/Fail Update** softkey. The text in grey indicates an inactive function (the pass/fail judgment is disabled).
- `Resync: On(0.4000)` - Indicates that the resynchronizing function is enabled and its threshold level is set to 0.4000. This field changes to `Resync: Off` when the **BERT Resync Off On** softkey is set to **Off** and the number in parentheses changes to display whatever value is set for the **BERT Resync Limits** softkey.
- `Clock Pol: Pos` - Indicates that the positive edge has been selected for the input polarity of the clock signal. This field changes to `Clock Pol: Neg` when the **Clock Polarity Neg Pos** softkey is set to **Neg**.
- `Data Pol: Pos` - Indicates that the data signal is used as it is for the data signal. This field changes to `Data Pol: Neg` when the **Data Polarity Neg Pos** softkey is set to **Neg**.
- `Clock Gate: On` - Indicates that the clock gate function is enabled. This field changes to `Clock Gate: Off` when the **Clock Gate Off On** softkey is set to **Off**.
- `Gate Pol: Pos` - Indicates that the clock signal is valid when the clock gate signal is high. This field changes to `Data Pol: Neg` when the **Data Polarity Neg Pos** softkey is set to **Neg**. The grey text in this field indicates an inactive function (the clock gate function is disabled).

- `Impedance: TTL` - Indicates that the TTL has been selected for the input termination mode. This field changes to `Impedance: 75 Ohm` when the **Impedance 75 Ohm TTL** softkey is set to **75 Ohm**.

2. Measurement Results

In this area, the measurement results are displayed. When the **Display Update Cycle End Cont** softkey is set to **Cycle End**, the measurement result is displayed only when the one measurement cycle has been completed. When the **Display Update Cycle End Cont** softkey is set to **Cont**, the intermediate measurement result is also displayed about every 200 ms during the measurement cycle.

NOTE You can select **Cont** only when the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps**.

- `Total Bits: 585792 Bits` - Shows the total bit count.
- `Error Bits: 5732 Bits` - Shows the error bit count.
- `BER: 0.97850432 %` - Shows the bit error rate measurement result. The BER measurement result can be displayed in percent or in the exponential format.

3. Other Information

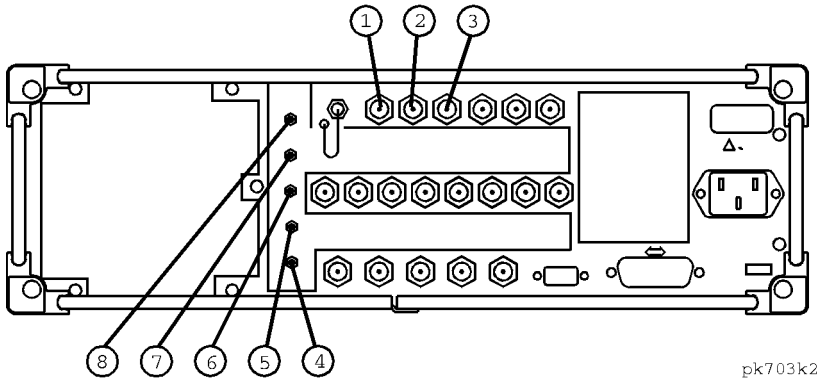
In this area, the measurement cycle counter is displayed on the right side. When the **Pass/Fail Off On** softkey is set to **On**, the result of the judgement is displayed in the center. The measurement error status may be displayed on the left side.

- `No Data` - In this field, `No Data` or `No Clock` may be displayed. `No Data` is displayed when there has been no data change for more than 200 clock signals. `No Clock` is displayed when there has been no clock input for more than 3 seconds.

  `Sync Loss` may be displayed under the `No Data` annunciator when the synchronization is lost. (It is not shown in this example.)

- `PASS` - In this field, the pass/fail judgement result is displayed when the **Pass/Fail Off On** softkey is set to **On**.
- `Cycle Counter: 7 / 12` - Indicates the current and total measurement cycle counts.

Rear Panel Overview



1. BER DATA IN Connector

Input the data streams for the bit error rate measurements. The rising (positive) or falling (negative) edge selected by the softkey or the GPIB command of the BER CLK IN signal is used to trigger the reading of the data. The connector type is a BNC (female). If you configure your instrument with Option 1EM, this input is changed from a BNC to an SMB.

2. BER CLK IN Connector

The rising (positive) or falling (negative) edge selected by the softkey or the GPIB command of the signal causes data on the BER DATA IN connector to be sampled. The connector type is a BNC (female). If you configure your instrument with Option 1EM, this input is changed from a BNC to an SMB.

3. BER GATE IN Connector

This connector can be enabled or disabled by the softkey or the GPIB command. Input the clock gate signal for the bit error rate measurements. The clock signal to the BER CLK IN connector is valid only when the signal to this connector is high or low which is selected by the softkey or the GPIB command. The connector type is a BNC (female). If you configure your instrument with Option 1EM, this input is changed from a BNC to an SMB.

4. BER MEAS END Connector

The BER MEAS END connector outputs the signal that indicates the status of the bit error rate (BER) measurements. BER measurements are being executed when the signal is high. The connector type is an SMB (female).

5. BER TEST OUT Connector

The BER TEST OUT connector outputs the signal that indicates the test result of the pass/fail judgment of the bit error rate measurements. The result is guaranteed at the falling edge of the signal of the MEAS END connector. The result is pass when the signal is low; the result is fail when the signal is high. The signal is also high when the pass/fail judgment is set to off. The connector type is an SMB (female).

6. BER ERR OUT Connector

The output of the BER ERR OUT connector is normally low. When the maximum data rate mode is set to 2 Mbps, the BER ERR OUT connector outputs the pulse signals that indicate the number of the error bits. One pulse whose width is about 80 ns indicates one error bit. Pulses for the error bits of one measurement cycle are not synchronized with the clock signal to the BER CLK IN connector, and are output during the signal of the BER MEAS END connector for the measurement cycle is high. The connector type is an SMB (female).

7. BER NO DATA Connector

The BER NO DATA connector outputs the signal that indicates the no data status. The no data status is reported when there has been no clock inputs for more than 3 seconds or there has been no data change for more than 200 bits. This signal is valid only when the signal of the BER MEAS END connector is high. No data status is detected when the signal is low. The connector type is an SMB (female).

8. BER SYNC LOSS Connector

The BER SYNC LOSS connector outputs the signal that indicates the synchronization loss state. This signal is only valid when the signal of the BER MEAS END connector is high. Synchronization loss state is detected when the signal is low. The connector type is an SMB (female).

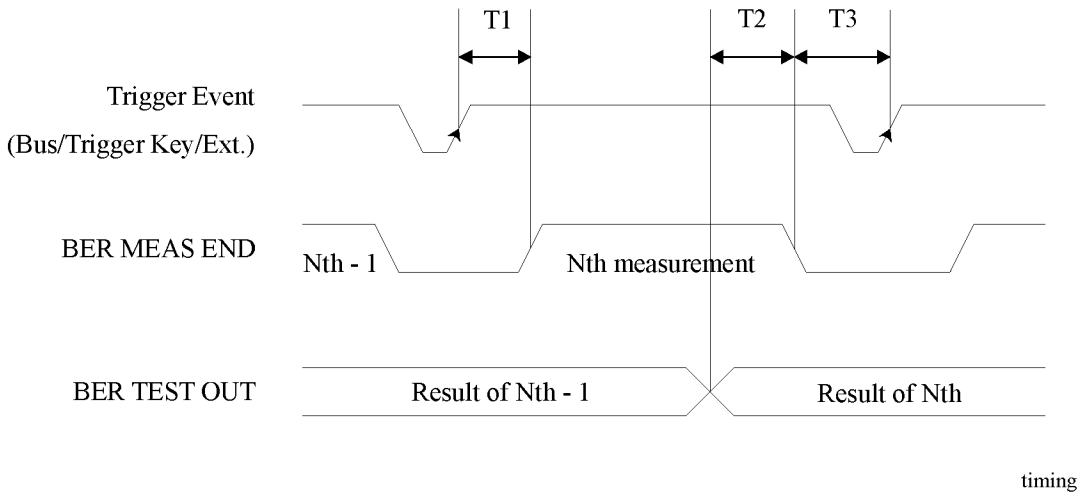
4 Operation

This section contains detailed information that will help you learn how to make bit error rate tests using your Agilent Technologies ESG Family Signal Generator with Option UN7.

Testing Signal Definitions

The following timing diagram shows the relationships between a trigger event and the output signals at the BER MEAS END and BER TEST OUT connectors.

Figure 4-1 Testing Signal Definitions



timing

- T1 is a firmware handling time measured from a Trigger event to the rising edge of a BER MEAS END signal.
- T2 is a firmware handling time measured from the falling edge of a BER TEST OUT signal to the falling edge of the BER MEAS END signal.
- T3 is a minimum requirement time measured from the falling edge of the BER MEAS END signal to the next trigger event. T3 should be greater than 0 second.

If a BER MEAS END signal stays high following a trigger event, the BER measurement is in progress and other trigger events are ignored. This state is stored in the status register and can be queried.

The pulse output of the BER TEST OUT for the Nth-1 test result ends prior to the falling edge of the BER MEAS END signal for the Nth measurement; so you can use this edge to start latching the Nth test result.

Functional Differences between Max. Data Rate 2 Mbps and 10 Mbps

Refer to the following summary list for the functional differences between the max. data rate 2 Mbps and 10 Mbps.

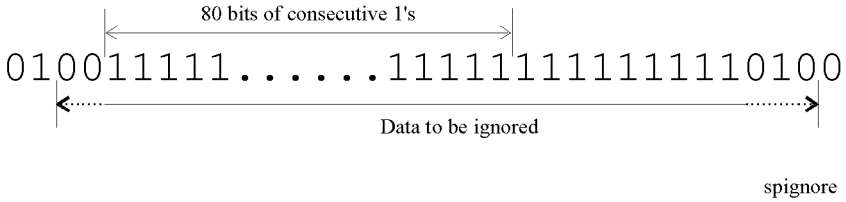
Table 4-1 Pattern Data Mode

Functions	2 Mbps	10 Mbps
Maximum Data Rate	Up to 2 Mbps	Up to 10 Mbps
Total Bit Count	100 to 4,294,967,295	
Intermediate result	Bit count, Error count, BER	Bit count
Maximum allowable BER for synchronization	Up to about 7%	Up to about 2%
Resynchronization	Supported	Not supported
Special pattern ignore	Supported	Not supported
BER OUTPUT ports	All ports are supported	BER ERR OUT is not supported

Data Processing

Special Pattern Ignore Function

The special pattern ignore function is especially useful for some radios which generate consecutive 0's or 1's data for TCH when they fail to detect the Unique Word or lose synchronization. If 80 consecutive incoming data bits are all either 1's or 0's, when the **Spcl Pattern Ignore Off On** softkey is set to **On**, all of the consecutive 0's or 1's (and several bits before and after the consecutive 0's or 1's) are ignored. The following figure shows the operation example of the special pattern ignore function.



spignore

Pass/Fail Judgement

There are two pass/fail judgement update modes: cycle end and fail hold. With cycle end selected, either pass or fail judgement is made for the results of each measurement cycle. With fail hold selected, the fail judgement is retained whenever a failure occurs during one loop of BER repeat measurements. Fail hold mode allows you to determine when a failure occurs at least once during an entire cycle of measurements.

Synchronization

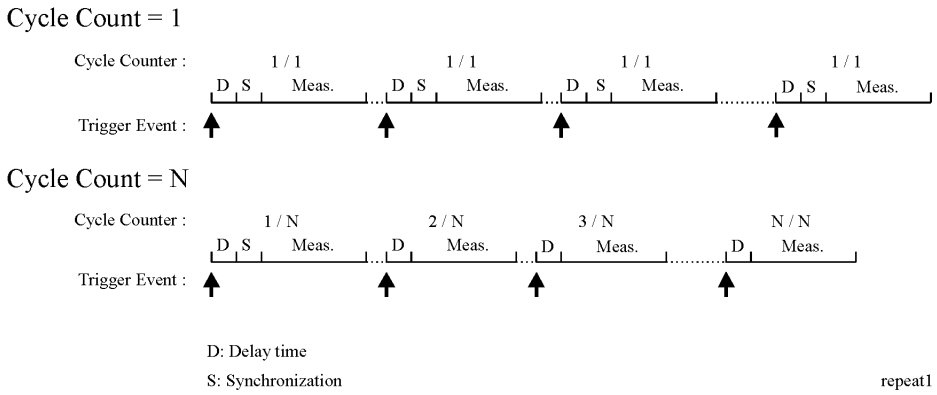
Immediately after the trigger event, the DSP for the BER measurement tries to establish synchronization using the first incoming bit stream. When the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **2Mbps**, 9 consecutive bits for PN-9 or 15 consecutive bits for PN-15 (not including any error bits) are required to initialize the register for the synchronization. When the **Max. Data Rate 2Mbps 10Mbps** softkey is set to **10Mbps**, 43 consecutive bits for PN-9 or 48 consecutive bits for PN-15 (not including any error bits) are required to initialize the register for the synchronization. In both cases, more bits are required to determine if synchronization has been established.

If the **Bit Delay Off On** softkey is set to **On**, the number of bits specified by the **Delayed Bits** are ignored. The synchronization checking is repeated using an error-free bit string, lengthened by the **Delayed Bits**, until synchronization is established.

When the **BERT Resync Off On** softkey is set to **On**, the BER measurements will be restarted if the intermediate BER measurement result exceeds the value specified by the **BERT Resync Limits**.

Repeat Measurements

When the **Cycle Count** softkey is set to more than 1, the synchronization performed before the start of each measurement is only executed the first time; then it keeps track of the clock signal and the PRBS generation for the incoming data. This function can reduce the total time for BER measurements. Also, once synchronization is established, it is retained even if the BER measurement result degrades. You may wish to adjust the signal level to find a specific BER value. However, once synchronization is lost in a repeat sequence, it will not be restored until the initiation of a new sequence. The following figure shows an example of the repeat measurements.

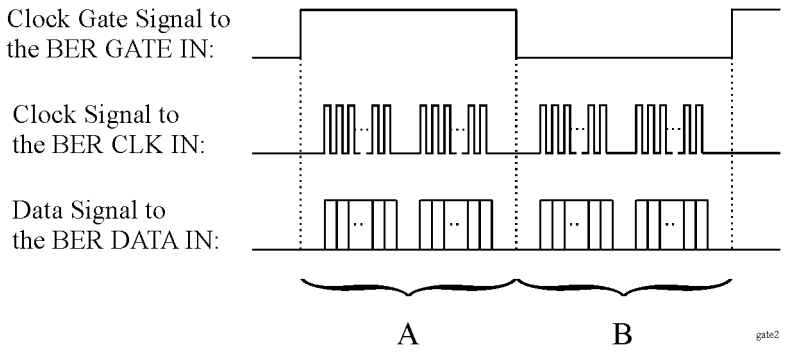


Clock Gate Function

When you use the clock gate function, the clock signal to the BER CLK IN connector is valid only when the clock gate signal to the BER GATE IN connector is ON.

Press the **Clock Gate Off On** softkey to toggle the clock gate function off and on.The **Clock Gate Polarity Neg Pos** softkey sets the input polarity of the clock gate signal supplied to the rear panel BER GATE IN connector. When you select **Pos** (positive), the clock signal is valid when the clock gate signal is high; when you select **Neg** (negative), the clock signal is valid when the clock gate signal is low.

The following figure shows an example of the clock gate signal.



- When the **Clock Gate Off On** softkey is set to **On**, and the **Clock Gate Polarity Neg Pos** softkey is set to **Pos**:

  The clock signal in “A” part is effective. Therefore, the bit error rate is measured using the clock and data signals in “A” part.

- When the **Clock Gate Off On** softkey is set to **On**, and the **Clock Gate Polarity Neg Pos** softkey is set to **Neg**:

  The clock signal in “B” part is effective. Therefore, the bit error rate is measured using the clock and data signals in “B” part.

- When the **Clock Gate Off On** softkey is set to **Off**:

  The clock signal in both “A” and “B” parts is effective. Therefore, the bit error rate is measured using the clock and data signal in both “A” and “B” parts.

5 Remote Programming

This chapter provides information about the BERT subsystem SCPI commands in alphabetical order. The descriptions include syntax requirements, ranges, restrictions, query responses, and status after *RST.

:CALCulate Subsystem SCPI Command Reference

The Calculate subsystem SCPI commands are used to set the controls and parameters associated with the display mode and the pass/fail judgement mode.

BER Display Mode

```
:CALCulate:BERT:DISPlay:MODE PERCent|SCIentific
:CALCulate:BERT:DISPlay:MODE?
```

This command selects the display mode for bit error rate measurement results. The choices are `PERCent` and `SCIentific`. When you select `PERCent`, BER measurement results are displayed in %. When you select `SCIentific`, BER measurement results are displayed in the following format: n.nnnnnE-mm (where n.nnnnn is a floating point part and E-mm is a power exponent part).

*RST value: Percent.

BER Display Update Mode

```
:CALCulate:BERT:DISPlay:UPDate CEND|CONT
:CALCulate:BERT:DISPlay:UPDate?
```

This command selects the display update mode during BER measurements. The choices are `CEND` (Cycle End) and `CONT` (Continuous). When you select `CEND`, the previous BER measurement result is displayed during the current measuring period. When you select `CONT`, the display shows its real-time intermediate results during each BER measurement.

*RST value: Cycle End.

BER Pass/Fail Judgement Mode

```
:CALCulate:BERT:COMParator:MODE CEND|FHOLd
:CALCulate:BERT:COMParator:MODE?
```

This command selects the pass/fail judgement mode of the comparator function. The choices are `CEND` (Cycle End) and `FHOLd` (Fail Hold). When you select `CEND`, each BER measurement result is compared with the Pass/Fail Limit value and judged to make a pass/fail test. When you select `FHOLd`, only one fail judgement is made once a fail has been found during that BER measurement loop. For automated tests, use the output signal from the rear panel BER TEST OUT port.

*RST value: Cycle End.

BER Pass/Fail Limits

```
:CALCulate:BERT:COMParator:THReshold <num>
:CALCulate:BERT:COMParator:THReshold?
```

This command specifies the threshold value for the pass/fail judgement function. This command is valid only while the BER pass/fail state command is ON (1). The range of the variable is from 0 to 1.

*RST value: 0.5.

BER Pass/Fail State

```
:CALCulate:BERT:COMParator[:STATe] ON|OFF|1|0
:CALCulate:BERT:COMParator[:STATe]?
```

This command enables and disables the pass/fail judgement function. The choices are `ON (1)` and `OFF (0)`. For automated tests, use the output signal from the rear panel BER TEST OUT port.

*RST value: Off.

:DATA Subsystem SCPI Command Reference

The data subsystem SCPI commands are used to read the measurement result value.

BER Measurement Result Query

`:DATA[:DATA]? BEC|BER|BITC|JUDGe|TBEC|TBER|TBIT`

This command queries the signal generator to return a measurement result value for the variable specified after the question mark. You can specify one of the following variables:

Parameter	Description	Type	Range
ALL	Synchronize intermediate values of Bit Error Count (BEC), Bit Error Rate (BER), and Bit Count (BITC)	Integer (BEC), Real (BER), Integer (BITC)	0 to BITC, 0 to 1, 0 to Total Bits
BEC	Intermediate Bit Error Count	Integer	0 to BITC
BER	Intermediate Bit Error Rate	Real	0 to 1
BITC	Intermediate Bit Count	Integer	0 to Total Bits
JUDGe	Pass/Fail result	String	FAIL or PASS
TBEC	Total Bit Error Count at the one measurement cycle end	Integer	0 to TBIT
TBER	Total Bit Error Rate at the one measurement cycle end	Real	0 to 1
TBIT	Total Bit Count at the one measurement cycle end	Integer	Total Bits

:INPut Subsystem SCPI Command Reference

The input subsystem SCPI commands are used to set the controls and the parameters associated with the input connectors for the bit error rate tests.

BER Clock Gate Polarity

```
:INPut:BERT:CGATe:POLarity POSitive|NEGative
:INPut:BERT:CGATe:POLarity?
```

This command selects the clock gate polarity. The choices are `POSitive` and `NEGative`. This clock gate signal is supplied to the rear panel BER GATE IN port. This command is valid only while the BER clock gate state is ON (1).

*RST value: Positive.

BER Clock Gate State

```
:INPut:BERT:CGATe[:STATe] ON|OFF|1|0
:INPut:BERT:CGATe[:STATe]?
```

This command enables and disables the clock gate function. The choices are `ON (1)` and `OFF (0)`.

*RST value: Off.

BER Clock Polarity

```
:INPut:BERT:CLOCk:POLarity POSitive|NEGative
:INPut:BERT:CLOCk:POLarity?
```

This command selects the clock polarity according to the clock signal supplied to the rear panel BER CLK IN port. The choices are `POSitive` and `NEGative`.

*RST value: Positive.

BER Data Polarity

```
:INPut:BERT:DATA:POLarity POSitive|NEGative
:INPut:BERT:DATA:POLarity?
```

This command selects the polarity of the data signal. The choices are `POSitive` and `NEGative`.

*RST value: Positive.

BER Input Impedance

```
:INPut:BERT:IMPedance OHM_75|TTL
:INPut:BERT:IMPedance?
```

This command selects the input impedance according to the input signals supplied to the rear panel BER DATA IN, BER CLK IN, and BER GATE IN ports. The choices are `OHM_75` (75 Ω) and `TTL`.

*RST value: TTL.

:SENSe Subsystem SCPI Command Reference

The sense subsystem SCPI commands are used to set the controls and parameters associated with the bit error rate measurements.

BER Cycle Count

```
:SENSe:BERT:TRIGger:COUNt <num>
:SENSe:BERT:TRIGger:COUNt?
```

This command specifies the repeat times of BER measurements. The range of the variable is from 1 to 65,535.

*RST value: 1.

BER Data Pattern

```
:SENSe:BERT:PRBS[:DATA] PN9|PN15
:SENSe:BERT:PRBS[:DATA]?
```

This command selects the data pattern for the incoming data bit stream to make BER measurements. The choices are PN9 and PN15.

*RST value: PN9.

BER Maximum Data Rate

```
:SENSe:BERT:PRBS:MDRate BPS_2M|BPS_10M
:SENSe:BERT:PRBS:MDRate?
```

This command selects the maximum data rate mode. The choices are `BPS_2M` (2 Mbps) and `BPS_10M` (10 Mbps). When you select 2 Mbps, all BERT functions are available for configuration. When you select 10 Mbps, the pass/fail judgement and special pattern ignore functions are unavailable.

*RST value: 2 Mbps.

BER Resync Limits

```
:SENSe:BERT:RSYNc:THReshold <num>
:SENSe:BERT:RSYNc:THReshold?
```

This command specifies the threshold level for the resynchronizing function. The range of the variable is from 0.05 to 0.40. This function is valid only when BERT resynchronization state is set to On.

*RST value: 0.40.

BER Resynchronization State

```
:SENSe:BERT:RSYNc[:STATe] ON|OFF|1|0
:SENSe:BERT:RSYNc[:STATe]?
```

This command enables and disables the resynchronization function. The choices are `ON (1)` and `OFF (0)`. This function is valid only when the maximum data rate is set to 2 Mbps.

*RST value: On.

BER Special Pattern Ignore Data

```
:SENSe:BERT:PRBS:FUNCtion:SPIGnore:DATA ALL_0|ALL_1
:SENSe:BERT:PRBS:FUNCtion:SPIGnore:DATA?
```

This command selects the bit parameter of the special pattern ignore function. The choices are `ALL_0` (All 0's) and `ALL_1` (All 1's). This command is valid only when Special Pattern Ignore state is already set to On.

*RST value: All 0's.

BER Special Pattern Ignore State

```
:SENSe:BERT:PRBS:FUNCtion:SPIGnore[:STATe] ON|OFF|1|0
:SENSe:BERT:PRBS:FUNCtion:SPIGnore[:STATe]?
```

This command enables and disables the operating state of the special pattern ignore function. The choices are `ON (1)` and `OFF (0)`. This function detects more than 80 bits of 0's or 1's in the incoming bit stream and ignores these bits when making BER measurements. This command is valid only when the maximum data rate is set to 2 Mbps.

*RST value: Off.

BER Total Bits

```
:SENSe:BERT:TBITs <num>
:SENSe:BERT:TBITs?
```

This command specifies the total bit count to be measured. The range of the variable is from 100 to 4,294,967,295.

*RST value: 10,000.

BER Trigger Bit Delay

```
:SENSe:BERT:TRIGger[:SOURce]:BDELay <num>
:SENSe:BERT:TRIGger[:SOURce]:BDELay?
```

This command specifies the number of delay bits for the trigger delay. The range of the variable is from 0 to 65,535. This function is valid only when the trigger bit delay state is set to On.

*RST value: 0.

BER Trigger Bit Delay State

```
:SENSe:BERT:TRIGger:BDELay:STATe ON|OFF|1|0
:SENSe:BERT:TRIGger:BDELay:STATe?
```

This command enables and disables the trigger bit delay function. The choices are `ON (1)` and `OFF (0)`.

*RST value: Off.

BER Trigger Source

```
:SENSe:BERT:TRIGger[:SOURce] BUS|EXTernal|IMMediate|KEY
:SENSe:BERT:TRIGger[:SOURce]?
```

This command selects the triggering type for starting BER measurements. The choices are `BUS` (trigger with a `*TRG` GPIB command), `EXTernal` (trigger with an external signal supplied to the rear panel TRIGGER IN connector), `IMMediate`, and `KEY` (trigger using the front panel **Trigger** key).

*RST value: Key.

BERT State

```
:SENSe:BERT:STATe ON|OFF|1|0
:SENSe:BERT:STATe?
```

This command enables and disables the BER measurement function. The choices are ON (1) or `OFF` (0).

*RST value: Off.

:STATus Subsystem SCPI Command Reference

The IEEE status subsystem is used to set the controls and the parameters associated with status conditions within the signal generator. For more information on the status register group and the data questionable BERT status group, refer to Chapter 1, "Preparing for Use," of the programming guide.

Status Preset

`:STATus:PRESet`

This command presets all transition filters, enable registers, and all error/event queue enable registers.

Data Questionable BERT Status Group Condition Register Query

`:STATus:QUEStionable:BERT:CONDition?`

This command returns the decimal value of the sum of the bits in the Data Questionable BERT Condition Register. For example, if no clock signal has been input for more than three seconds during the bit error rate measurements (bit 0), then a value of 1 is returned. Note that the data in this register is continuously updated and reflects the current conditions.

Data Questionable BERT Status Group Enable

`:STATus:QUEStionable:BERT:ENAble <num>`

This command determines which bits in the Data Questionable BERT Status Group Event Register will set the Data Questionable BERT Summary bit (bit 12) in the Data Questionable Status Group Condition Register. The variable `<num>` is the sum of the decimal values of the bits you want to enable.

Data Questionable BERT Status Group Event Register Query

`:STATus:QUEStionable:BERT[:EVENt]?`

This command returns the decimal value of the sum of the bits in the Data Questionable BERT Event Register. For example, if no clock signal for the bit error rate tests has been input for more than three seconds (bit 0), then a 1 is returned. Note that the register requires that the equivalent PTR or NTR filters be set before a condition register bit can set a bit in the Event register. Note also that the data in this register is latched until it is queried. Once queried, the data is cleared.

Data Questionable BERT Status Negative Transition Filter Register Enable

`:STATus:QUEStionable:BERT:NTRansition <num>`

This command determines which bits in the Data Questionable BERT Status Group Condition Register will set the corresponding bit in the Data Questionable BERT Status Group Event Register when that bit has a negative transition (1 to 0). The variable <num> is the sum of the decimal values of the bits that you want to enable.

Data Questionable BERT Status Positive Transition Filter Register Enable

`:STATus:QUEStionable:BERT:PTRansition <num>`

This command determines which bits in the Data Questionable BERT Status Group Condition Register will set the corresponding bit in the Data Questionable BERT Status Group Event Register when that bit has a positive transition (0 to 1). The variable <num> is the sum of the decimal values of the bits that you want to enable.

:TRIGger Subsystem SCPI Command Reference

The trigger subsystem is used to set the controls and parameters associated with triggering a BER measurement.

Abort

`:ABORt`

There is no query for this command.

This command causes the sweep in progress to abort, then resets the sweep. This command can also cause the BER measurement in progress to abort, and then set the BER measurement state to Off. The pending operation flag (affecting `*OPC`, `*WAI`, and `*OPC?`) will undergo a transition once the sweep or BER measurement has been reset.

6 Programming Command Cross-Reference

This chapter lists BERT softkeys and their corresponding SCPI programming commands.

Mode - BERT Softkeys

Key	SCPI Command
BERT Off On	:SENSe:BERT:STATe ON|OFF|1|0 :SENSe:BERT:STATe?
BERT Resync Off On	:SENSe:BERT:RSYNc[:STATe] ON|OFF|1|0 :SENSe:BERT:RSYNc[:STATe]?
BERT Trigger	:SENSe:BERT:TRIGger[:SOURce] IMMediate|KEY|BUS|EXTernal :SENSe:BERT:TRIGger[:SOURce]?
Bit Delay Off On	:SENSe:BERT:TRIGger:BDELay:STATe ON|OFF|1|0 :SENSe:BERT:TRIGger:BDELay:STATe?
Bus	:SENSe:BERT:TRIGger[:SOURce] BUS :SENSe:BERT:TRIGger[:SOURce]?
Clock Gate Off On	:INPut:BERT:CGATe[:STATe] ON|OFF|1|0 :INPut:BERT:CGATe[:STATe]?
Clock Gate Polarity Neg Pos	:INPut:BERT:CGATe:POLarity NEGative|POSitive :INPut:BERT:CGATe:POLarity?
Clock Polarity Neg Pos	:INPut:BERT:CLOCk:POLarity NEGative|POSitive :INPut:BERT:CLOCk:POLarity?
Cycle Count	:SENSe:BERT:TRIGger:COUNt <num> :SENSe:BERT:TRIGger:COUNt?
Cycle End	:CALCulate:BERT:COMParator:MODE CEND :CALCulate:BERT:COMParator:MODE?
Data	:SENSe:BERT:PRBS[:DATA] PN9|PN15 :SENSe:BERT:PRBS[:DATA]?
Data Polarity Neg Pos	:INPut:BERT:DATA:POLarity NEGative|POSitive :INPut:BERT:DATA:POLarity?
Delayed Bits	:SENSe:BERT:TRIGger:BDELay <num> :SENSe:BERT:TRIGger:BDELay?
Display BER % Exp	:CALCulate:BERT:DISPlay:MODE PERCent|SCIentific :CALCulate:BERT:DISPlay:MODE?
Display Update Cycle End Cont	:CALCulate:BERT:DISPlay:UPDate CEND|CONT :CALCulate:BERT:DISPlay:UPDate?

Key	SCPI Command
Ext	:SENSe:BERT:TRIGger[:SOURce] EXTernal :SENSe:BERT:TRIGger[:SOURce]?
Fail Hold	:CALCulate:BERT:COMParator:MODE FHOLd :CALCulate:BERT:COMParator:MODE?
Immediate	:SENSe:BERT:TRIGger[:SOURce] IMMediate :SENSe:BERT:TRIGger[:SOURce]?
Impedance 75 Ohm TTL	:INPut:BERT:IMPedance OHM_75|TTL :INPut:BERT:IMPedance?
Max. Data Rate 2Mbps 10Mbps	:SENSe:BERT:PRBS:MDRate BPS_2M|BPS_10M :SENSe:BERT:PRBS:MDRate?
Pass/Fail Limits	:CALCulate:BERT:COMParator:THReshold <num> :CALCulate:BERT:COMParator:THReshold?
Pass/Fail Off On	:CALCulate:BERT:COMParator[:STATe] ON|OFF|1|0 :CALCulate:BERT:COMParator[:STATe]?
Pass/Fail Update	:CALCulate:BERT:COMParator:MODE CEND|FHOLd :CALCulate:BERT:COMParator:MODE?
PN9	:SENSe:BERT:PRBS[:DATA] PN9 :SENSe:BERT:PRBS[:DATA]?
PN15	:SENSe:BERT:PRBS[:DATA] PN15 :SENSe:BERT:PRBS[:DATA]?
Resync Limits	:SENSe:BERT:RSYNc:THReshold <num> :SENSe:BERT:RSYNc:THReshold?
Special Pattern 0's 1's	:SENSe:BERT:PRBS:FUNCtion:SPIGnore :DATA ALL_0|ALL_1 :SENSe:BERT:PRBS:FUNCtion:SPIGnore:DATA?
Special Pattern Ignore Off On	:SENSe:BERT:PRBS:FUNCtion:SPIGnore[:STATe] ON| OFF|1|0 :SENSe:BERT:PRBS:FUNCtion:SPIGnore[:STATe]?
Total Bit	:SENSe:BERT:TBITs <num> :SENSe:BERT:TBITs?
Trigger Key	:SENSe:BERT:TRIGger[:SOURce] KEY :SENSe:BERT:TRIGger[:SOURce]?

7 Programming Examples

The following section includes a programming example to help you understand how to build automated tests using the bit error rate test.

Testing Bit Error Rate on a PHS radio

In this example, the signal generator is configured to the initial settings of a PHS π/4 DQPSK Modulation Sensitivity Bit Error test. The carrier frequency is set to 1.89515 GHz at -100 dBm. PRBS data type is PN9 with the max. data rate of 2 Mbps. BERT Total Bit is set to 10,000. BERT Trigger is set to Bus.

CLEAR and RESET the controller, type the following commands and RUN the program.

```
10 !******************************************************
20 !
30 ! PROGRAM NAME:   BERT.BAS Rev. A.01.00
40 !
50 ! PROGRAM DESCRIPTION:  In this example, the signal generator is
60 ! configured to the initial settings of a PHS Pi/4 DQPSK
70 ! modulation sensitivity bit error test.  The carrier is a
80 ! frequency of 1.89515 GHz at -100 dBm. PRBS data type is PN9 with
90 ! the max. data rate of 2 Mbps. BERT Total Bit is set to 10,000.
100 ! BERT Trigger is set to Bus.
110 !
120 ! CLEAR and RESET the controller, and type the following commands and RUN
130 ! the program:
140 !
150 !******************************************************
160 !
170 Sig_gen=719
180 LOCAL Sig_gen
190 CLEAR Sig_gen
200 CLEAR SCREEN
210 OUTPUT Sig_gen;"*RST"
220 OUTPUT Sig_gen;"*CLS"
230 ! ****************************************
240 OUTPUT Sig_gen;"RAD:PHS:FCH 1"
250 OUTPUT Sig_gen;"RAD:PHS:BURS:STAT ON"
260 OUTPUT Sig_gen;"RAD:PHS:DLIN:SLOT1:TYP TCH"
270 OUTPUT Sig_gen;"RAD:PHS:DLIN:SLOT1:STAT ON"
280 OUTPUT Sig_gen;"RAD:PHS:STAT ON"
290 OUTPUT Sig_gen;"POW -100 dBm"
300 OUTPUT Sig_gen;"OUTP ON"
310 ! ****************************************
320 INPUT "Set the UUT to the RX mode, then press [Enter].",Dummy$
330 ! ****************************************
340 OUTPUT Sig_gen;"SENS:BERT:PRBS PN9"
350 OUTPUT Sig_gen;"SENS:BERT:PRBS:MDR BPS_2M"
360 OUTPUT Sig_gen;"SENS:BERT:TBIT 10000"
370 OUTPUT Sig_gen;"SENS:BERT:STAT ON"
380 OUTPUT Sig_gen;"SENS:BERT:TRIG BUS"
390 OUTPUT Sig_gen;"*TRG"
400 ! ****************************************
410 WAIT 0.2
420 REPEAT
430 OUTPUT Sig_gen;"STAT:OPER:COND?"
440 ENTER Sig_gen;Bert_stat
450 UNTIL BIT(Bert_stat,4)=0
460 ! ****************************************
470 OUTPUT Sig_gen;"DATA? TBER"
480 ENTER Sig_gen;A
490 PRINT "BER:",A
500 ! ****************************************
510 LOCAL Sig_gen
```

```
520 DISP "Press RUN to start again."
530 END
```

Program Comments

10 to 160:	Title and program description
170:	Assigns the signal generator's GPIB address to a variable.
180 to 200:	Sets the signal generator in LOCAL mode, and clears the controller's display.
210:	Sets the signal generator to a defined state for programming.
220:	Clears the signal generator's Status Byte Register.
230:	Program border
240:	Sets the signal generator's output frequency channel number of PHS to 1 (1.89515 GHz).
250:	Turns on the signal generator's frame burst.
260:	Configures the downlink timeslot 1 as a traffic channel type.
270:	Turns on the timeslot 1.
280:	Enables PHS modulation.
290:	Sets the signal generator's output carrier power to -100 dBm.
300:	Turns on the RF output power.
310:	Program border
320:	Waits until the UUT is set to the receiver mode.
330:	Program border
340:	Sets the BERT PRBS data type to PN9.
350:	Sets the BERT PRBS data rate to 2 Mbps.
360:	Sets the BERT total bit to 10,000.
370:	Enables the BERT function.
380:	Sets the BERT trigger source to Bus.
390:	Sends the bus trigger via GPIB.
400:	Ends the program.
410:	Waits for 0.2 second for firmware processing.
420:	Repeats the following program lines.
430:	Queries the signal generator's operating condition status.
440:	Enters the query's response.

450:	Determines when a BER measurement is completed.
460:	Program border
470:	Queries the signal generator for the BER data.
480:	Enters the BER data into the register A.
490:	Prints the BER data on the controller's screen.
500:	Program border
510:	Returns the signal generator to local.
520:	Prints a message on the controller's display.
530:	Ends this program.

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